REMARKS

Claims 34-44 and 53-56 are pending in the application. Claims 34-44 and 53-56 stand rejected. Claims 34-40 and 53-56 have been amended. In view of the amendments to the claims and the following remarks, Applicants respectfully request the rejections be withdrawn and the claims allowed.

Claims 34-44 and 53-56 stand rejected under 35 U.S.C. § 112, first paragraph, for failure to comply with the written description requirement. Specifically, the Examiner alleges that a claim limitation recently added to claims 34 and 53 lacks support from the original disclosure. The disputed limitation in both claims is that "said second presence detect information [is] related to only said semiconductor memory device." In response to this rejection and in order to further prosecution of the application, Applicants have amended claims 34 and 53 to address the Examiner's concerns. Applicants respectfully request the rejection be withdrawn.

Claims 34-40 and 53-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,092,146 to Dell et al. ("Dell") in view of U.S. Patent No. 4,625,162 to Bosnyak ("Bosnyak"). The rejection is respectfully traversed.

Claim 34 recites a signaling circuit for encoding presence detect data. The signaling circuit comprises "a first signal encoding portion for encoding first presence detect information" and "a second signal encoding portion for encoding second presence detect information." Both the first and the second presence detect information relate to "a random access semiconductor memory chip." The first presence detect information is "disposed in a hardwired circuit of said random access semiconductor memory chip during the manufacturing of said random access semiconductor memory chip." The second presence detect information is "disposed in a programmable circuit of said random access semiconductor memory chip." Applicants respectfully submit

that the cited references do not disclose, teach or suggest each of the limitations recited in claim 34. Specifically, the cited references do not disclose presence detect data related to a random access semiconductor memory chip wherein the presence detect data is either "disposed in a hardwired circuit of said random access semiconductor memory chip" or "disposed in a programmable circuit of said random access semiconductor memory chip."

Applicants refer the Examiner to Figure 2A of the present application, shown below, to further illustrate the meaning of the limitations recited by claim 34. Figure 2A depicts a memory module 18A which supports multiple memory chips 30A-H. The memory module 18A can be, for example, a single in-line memory module (SIMM), a dual in-line memory module (DIMM), a small outline dual in-line memory module (SO-DIMM) or another type of memory module. Application, ¶ [0028]. The memory chips 30A-H can be, for example, dynamic random access memory (DRAM) chips. Application, ¶ [0030]. "In contrast to prior memory modules, the module 18A does not require a separate integrated chip to provide presence detect signals to identify the memory configuration of either the module or the memory chips 30A through 30H. Rather, as shown in the implementation of FIG. 2A, each of the memory chips 30A through 30H includes logic 40 for storing presence detect information and for allowing the presence detect data to be accessed selectively for transmission over the data line 22. The logic 40 is incorporated into the integrated circuit which forms each respective memory chip 30A through 30H. Thus, each memory chip, such as the memory chip 30A, can store presence detect data which can be provided to the memory controller 14 over the data line 22 in response to a control signal received on the control line 23." Application, ¶ [0031].

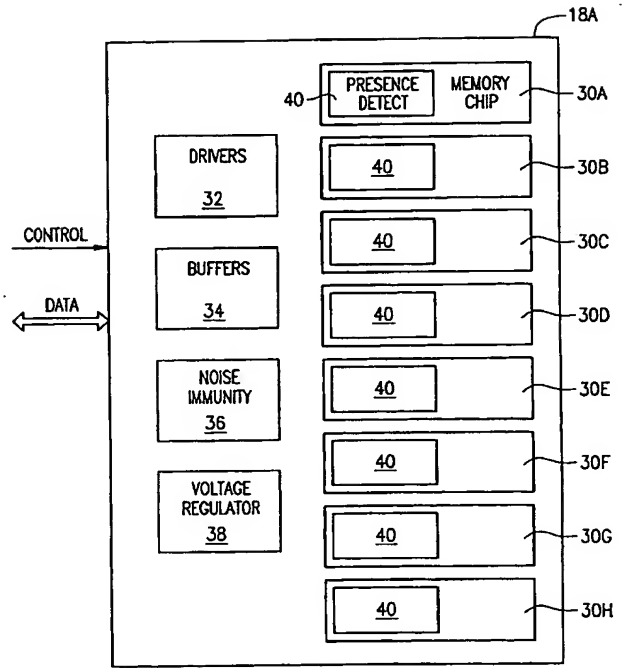

FIG. 2A

Dell, however, has nothing to do with either hardwiring or programming serial presence detect data onto random access semiconductor memory chips, such as DRAMs. As shown in Figure 3 of Dell (reproduced below), Dell is instead directed to a memory adapter 100 for configuring traditional SIMMs 202, 204 in a computer system that normally employs DIMMs. Dell, col. 1, line 66, col. 2, lines 1-2. The adapter includes a programmable logic device 114 for interrogating and configuring serial presence detect data. Dell, col. 2, lines 2-15. The programmable logic device 114 configures the serial presence detect data received from the SIMMs 202, 204 by programming an EEPROM 106 whose purpose is to store the serial presence detect data. Dell, col. 2, lines 4-5, 13-15. In other words, the programmable logic device 114 outputs serial presence detect data to the EEPROM 106, which then stores the data. *Id.* The programmable logic device 114 has certain output bits that are factory set. Dell, col. 5, lines 22-23. Other output bits of the programmable logic device 114 are

determined by SIMM 202, 204 and DIP switch 108, 110 inputs. Dell, col. 5, lines 23-24. The programmable logic device outputs are used to program the EEPROM 106 with the serial presence detect data to allow a computer system to access the SIMMs 202, 204. Dell, col. 5, lines 8-14. In Dell, the EEPROM 106 may be programmed each time that a power-on-reset occurs. *See* Dell, Fig. 5.

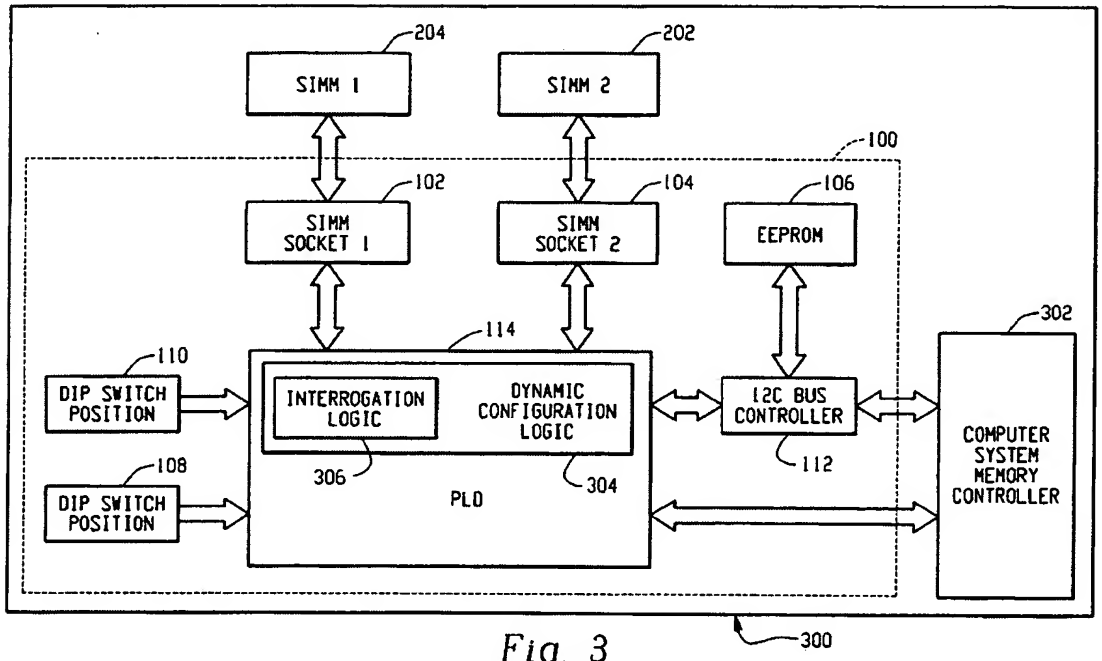

Fig. 3

Applicants respectfully submit that neither the Dell EEPROM 106, the Dell programmable logic device 114, nor the Dell adapter module 100 include or suggest each of the elements and limitations recited by claim 34. Claim 34 recites first and second signal encoding portions for encoding presence detect information on a random access semiconductor memory chip. Dell fails to show a random access semiconductor memory chip. Although one skilled in the art would recognize that the SIMM modules

in Dell include random access semiconductor memory chips, Dell does not teach or even suggest that these chips also include presence detect logic on the chips.

The focus of Dell is instead on an adapter module that includes an EEPROM for storing presence detect information. The Dell EEPROM is not, by definition, a random access semiconductor memory chip. Additionally, although the Dell EEPROM may be said to be a programmable circuit in which presence detect data is stored, the Dell EEPROM is not a hardwired circuit for storing presence detect data. The Dell EEPROM is a completely reprogrammable device. In fact, the Dell EEPROM may be reprogrammed each time a power-on-reset occurs. Dell, Fig. 5. By the very nature of an EEPROM, an EEPROM is programmed after manufacture. EEPROMs are designed to allow reprogramming after manufacture, and Dell teaches nothing different. In other words, the Dell EEPROM cannot include both a first signal encoding portion and a second signal encoding portion, wherein the first signal encoding portion encodes information that is "disposed in a hardwired circuit of said random access semiconductor memory chip *during the manufacturing of said random access semiconductor memory chip*," as recited by claim 34 (emphasis added). Dell does not teach such a specialized EEPROM device. Additionally, the presence detect data stored on the EEPROM does not relate to the EEPROM, but instead relates to the memory chips on the SIMM modules. Claim 34 recites a signal encoding portion that encodes presence detect information on the random access semiconductor memory chip for which the presence detect information relates.

The Dell programmable logic device also fails to read on the elements recited by claim 34. The Dell programmable logic device includes output bits that are determined according to certain preprogrammed characteristic tables of the programmable logic device. Dell, col. 2, lines 11-13, Table 1. According to Table 1 of Dell, certain serial presence detect data bytes are factory set. Other output bits of the

programmable logic device are determined by SIMM and DIP switch inputs. Dell, col. 5, lines 23-24. The SIMM and DIP switch inputs cause the programmable logic device to output serial presence detect data according to its preprogrammed tables. The serial presence detect data stored in the tables of the programmable logic device is not, however, related to the programmable logic device, and neither can the programmable logic device be described as a random access semiconductor memory chip. The presence detect data stored in the tables is related to multiple SIMMs, thus allowing a user to select among the multiple SIMM devices to be used. *See* Dell, Tables 2.1, 2.2, 3.1, 3.2, 4.1, 4.2, 4.3. In other words, the Dell programmable logic device does not include "presence detect information relating to a random access semiconductor memory chip" upon which said presence detect information is disposed.

In addition, Dell does not disclose, teach or suggest that its memory adapter is "a random access semiconductor memory chip" as recited in claim 34. The Dell EEPROM and the Dell programmable logic device are located on a memory adapter, and are not a part of a random access semiconductor memory chip. Although the functions of the EEPROM and the programmable logic device might be combinable as a single integrated circuit, there is no suggestion to do so or, moreover, to combine their features into a portion of a random access semiconductor memory chip.

Bosnyak also fails to remedy the shortcomings of Dell. Bosnyak is directed to the simultaneous testing of a plurality of fuses in a fusible link array. Bosnyak, col. 2, lines 9-11. Bosnyak is relied upon by the Examiner to teach that array bits may be set to one of two logical states by either keeping the bit fuse intact (thus creating a short circuit) or by blowing the fuse to create an open circuit. Office Action, p. 4. However, Bosnyak does nothing to correct Dell's deficiencies. Specifically, Bosnyak does nothing to show how the Dell EEPROM, the Dell programmable logic device and the Dell memory adapter module can include "presence detect information relating to a random

access semiconductor memory chip" upon which said information is disposed in both programmable and hardwired circuits. Bosnyak fails to show how the EEPROM, the programmable logic device and the memory adaptor are random access semiconductor memory chips.

For at least the foregoing reasons, Applicants respectfully submit that claim 34 is allowable over the combination of Dell and Bosnyak. Claims 35-40 depend from claim 34 and are allowable along with claim 34 for at least the reasons set forth above and on their own merits.

Claim 53 recites a method of operating a random access semiconductor memory chip. The method includes the act of "receiving a first signal at a memory controller from said random access semiconductor memory chip, said first signal encoding first presence detect information relating to said random access semiconductor memory chip, said first presence detect information being hardwired into said random access semiconductor memory chip during manufacturing of said random access semiconductor memory chip." The method of claim 53 also includes "receiving a second signal at a memory controller from said random access semiconductor memory chip, said second signal encoding second presence detect information relating to said random access semiconductor memory chip, said second presence detect information being programmed into said random access semiconductor memory chip subsequent to manufacturing of said random access semiconductor memory chip." Applicants respectfully submit that the combination of Dell and Bosnyak fails to teach or suggest the receipt of a signal encoding first presence detect information hardwired into a random access semiconductor memory chip and a signal encoding second presence detect information programmed into the random access semiconductor memory chip, as recited in claim 53 and as explained above. As such, claim 53 is allowable over the combination of Dell and Bosnyak. Claims 54-56 depend

from claim 53 and are allowable along with claim 53 for at least the reasons set forth above and on their own merits.

Applicants respectfully request that the rejection be withdrawn and claims 34-40 and 53-57 be allowed.

Claims 41-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell in view of Bosnyak. The rejection is respectfully traversed.

Claims 41-44 depend from claim34 and are allowable along with claim 34 for at least the reasons set forth above and on their own merits. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 34-44 and 53-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell in view of Bosnyak. The rejection is respectfully traversed. Because the combination of Dell and Bosnyak fails to teach or suggest each of the elements and limitations of independent claims 34 and 53, as explained above, claims 34 and 53 are allowable. Claims 35-44 depend from claim 34, and are also allowable for at least the same reasons and on their own merits. Claims 54-56 depend from claim 53, and are also allowable for at least the same reasons and on their own merits. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 34-44 and 53-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell in view of Bosnyak, and further in view of U.S. Patent No. 6,275,259 to Gowda et al. ("Gowda"). The rejection is respectfully traversed.

Claim 34 recites, among other things, a signaling circuit for encoding presence detect data. The signaling circuit comprises "a first signal encoding portion for encoding first presence detect information" and "a second signal encoding portion

for encoding second presence detect information." The first presence detect information is "disposed in a hardwired circuit of a random access semiconductor memory chip during the manufacturing of said random access semiconductor memory chip." The second presence detect information is "disposed in a programmable circuit of said random access semiconductor memory chip." As set forth above, the combination of Dell and Bosnyak fails to disclose, teach or suggest these limitations (as well as others mentioned above). Applicants respectfully submit that Gowda, which has been cited as teaching hardwiring circuitry, also fails to disclose, teach or suggest these limitations.

As such, the cited combination fails to disclose, teach or suggest the limitations of claim 34. Claims 35-40 depend from claim 34 and are allowable along with claim 34 for at least the reasons set forth above and on their own merits. Applicants also respectfully submit that claim 53 is allowable over the combination of Dell, Bosnyak and Gowda for at least the reasons set forth above. Claims 54-56 depend from claim 53 and are allowable along with claim 53 for at least the reasons set forth above and on their own merits.

Accordingly, the rejection should be withdrawn and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Dated: April 21, 2006

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant